(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
10 February 2005 (10.02.2005)

PCT

(10) International Publication Number
WO 2005/013053 A2

(51) International Patent Classification[7]: G06F

(21) International Application Number: PCT/US2004/023689

(22) International Filing Date: 23 July 2004 (23.07.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/490,180 25 July 2003 (25.07.2003) US

(71) Applicant and
(72) Inventor: **ZINGHER, Arthur, R.** [US/US]; 8332 Regents Rd., Apt 2E, San Diego, CA 92122-1313 (US).

(74) Agent: **KOLEGRAFF, William, J.**; 3119 Turnberry Way, Jamul, CA 91935 (US).

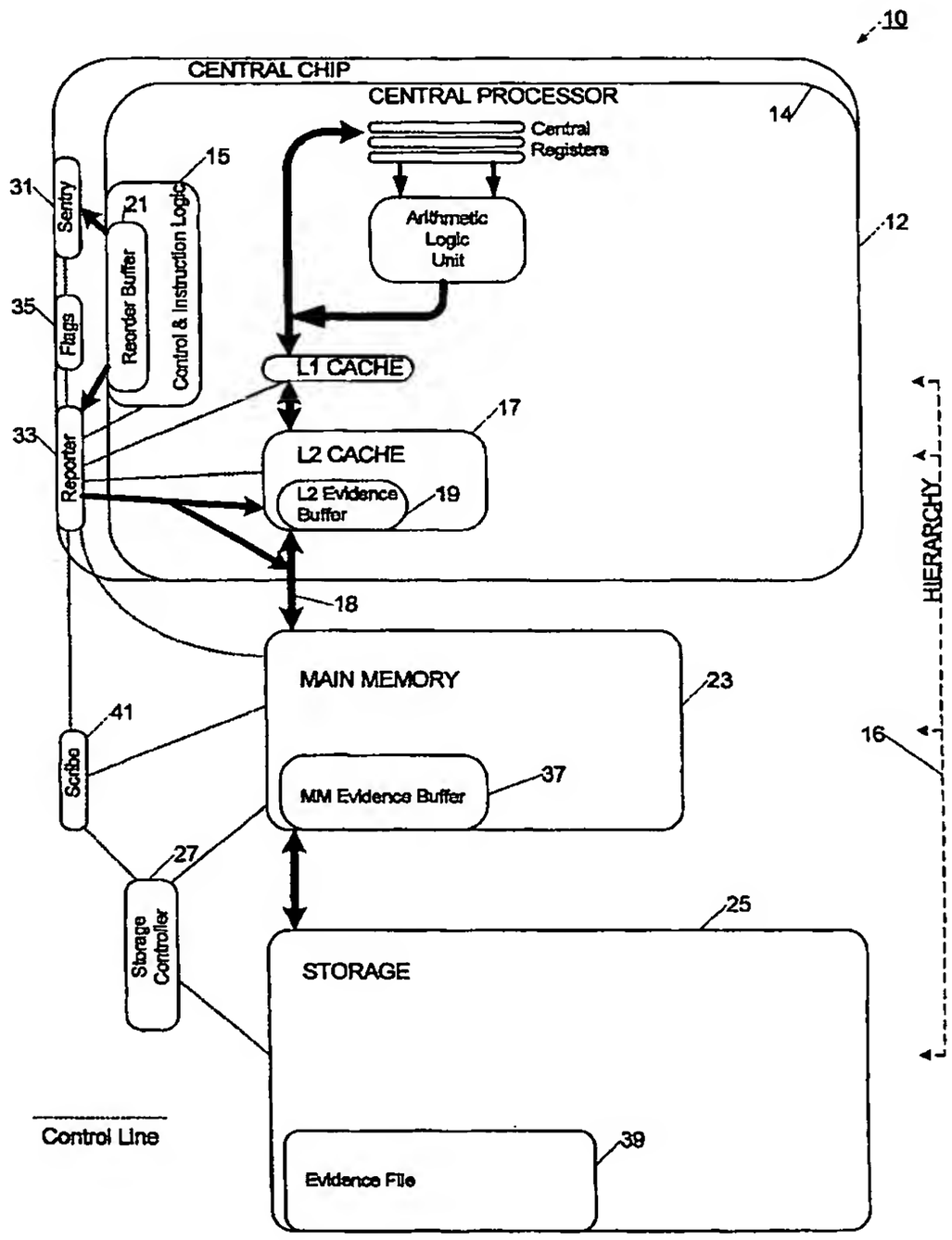
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:
— *of inventorship (Rule 4.17(iv)) for US only*

[Continued on next page]

(54) Title: APPARATUS AND METHOD FOR SOFTWARE DEBUGGING



(57) **Abstract:** The software debugging system provides a processor that is executing a software process, and the software process has a bug or other failure. A fast-response reporter circuit connects to a low level asset in the processor, such as a reorder buffer, commit buffer, or high speed data path. The fast response reporter circuit is configured to selectively extract data from the low-level asset, and the extracted data is transmitted to an evidence file for review and analysis. In one arrangement, a fast-response sentry circuit also connects to a low-level asset in the processor, and is configured to monitor for a predefined event. When the predefined event occurs, the fast-response sentry circuit causes an action to occur, such as activation of the reporter fast-response circuit.

WO 2005/013053 A2

Published:

— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.